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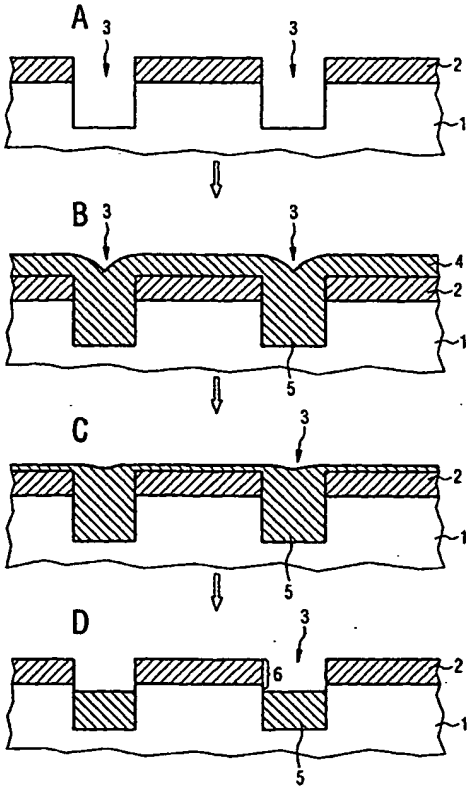
(54) Title: PROCESS FOR PLANARIZATION AND RECESS ETCHING OF POLYSILICON IN AN OVERFILLED TRENCH



(57) Abstract: The invention is directed to a process for forming a recess in at least one poly silicon overfilled trench in an integrated circuit, comprising the following steps: uniformly etching the poly silicon overfill layer (4); stopping the etching before the poly silicon layer (4) is completely removed from the surface of the integrated circuit; and recess etching the polysilicon layer (4) with microtrenching properties for forming a substantially planar recess (6) near the top of the at least one trench (3).

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Description

PROCESS FOR PLANARIZATION AND RECESS ETCHING OF POLYSILICON IN AN OVERFILLED TRENCH

For a number of uses, e.g. for the fabrication of capacitors within integrated circuits, cavities are created in the lower layer of the circuit. Such cavities are generally called trenches. In the case of the formation of a capacitor, such cavity is also called a deep trench.

Conventionally, a trench is formed in the single crystal silicon and then later filled with poly silicon which is deposited onto the entire surface of the wafer containing the integrated circuit and including the trench. This is done, for example with a low pressure chemical vapour deposition process. The deposition leads to a layer which completely fills the trench. To ensure that the trench is completely filled, the trench is overfilled which leads to a poly silicon layer with minor indentations which indicate the location of the trenches.

After deposition of the poly silicon, the excessive poly silicon must be removed. This is conventionally done by two process steps which are called Planarization and Recess etch. In the first step, a CMP process is utilised to remove any poly silicon from the uppermost surface. In order to not impair the structure of the silicon, a nitride layer is provided which is deposited onto the silicon prior to the formation of the trench. This nitride layer acts as an etch and polish stop layer. The CMP planarization is processed with a fixed time. This provides the opportunity to overpolish the poly silicon. Next, the recess etch step, a plasma etch pro-

cess, is used to remove some of the poly silicon from within the trenches.

This known process has a severe disadvantage, though. While all other poly silicon planarizations employed in the manufacturing of integrated circuits can be done within integrated processes, the CMP process of this planarization has to be handled separately. This complicates the planarization, increases risk to damages and results in higher cost.

U.S. Patent 5,252,506 discloses a method for etching a trench filled with poly silicon. The poly silicon top layer is first etched with SF6/He in a timed etch process. The resulting structure is followed by patterning of the poly silicon top layer to create openings. An additional patterning step occurs by coating, exposing and development of a resist. Finally, a two step poly overetch follows using SF6/He in the first step and Cl1/He in the second step.

In the article Shrinath Ramaswami et al.: "Polysilicon Planarization Using Spin-On Glass", Journal of the Electrochemical Society, Vol. 139, No. 2, February 1, 1992, pages 591 - 599 a trench filled with poly silicon is first coated with spin-on glass using carbone/fluorine etch chemistry with changing C/F-ratios.

It is therefore the object of the present invention to modify this planarization step and the recess etch step in order to arrive at a process which can be better integrated.

This object is solved by the provision of a process according to independent claim 1. Further advantageous features, as-

pects and details of the invention can be derived from the dependent claims, the description, and the drawings.

Process for forming a recess in at least one poly silicon overfilled trench in an integrated circuit, comprising the following steps: uniformly etching the poly silicon overfill layer using a gas mixture comprising SF6 and CF4; stopping the etching before the poly silicon layer is completely removed from the surface of the integrated circuit; and recess etching the poly silicon layer with microtrenching properties using a gas mixture comprising hydrogen bromine and chlorine for forming a substantially planar recess near the top of the at least one trench.

By the process according to the invention, the CMP process step which was hitherto necessary, can be entirely avoided. The inventive process allows an integrated approach, so that an interruption is no longer needed.

The etching step may comprise a plasma etching. In general, this step will be performed as any plasma etching commonly known to be suitable for etching poly silicon layers, e.g. with a high density plasma etch tool, i.e. a particular kind of plasma chamber.

The time to stop the etching is preferably determined based on measuring the layer thickness of the poly silicon layer. By monitoring the thickness of the remaining poly silicon layer, the inventive process can be fine tuned to achieve the desired aim.

Such measuring of the thickness of the poly silicon layer can be performed by interference spectrometry which allows a pre-

cise measurement of the thickness. The interference spectroscopy uses the reflection of the emitted waves from surfaces. Throughout the etching process, when the thickness of the poly silicon layer decreases below a certain threshold, the layer becomes transparent for the incident light which is then also partly reflected from the next surface, e.g. the base silicon or a further layer overlaying this silicon.

Such a further layer may be a nitride layer which is interposed between the silicon of the integrated circuit and the poly silicon layer. Depositing such a layer on the surface of the silicon is in fact a routine measure in order to protect the silicon from undesired degradation throughout the manufacturing steps of integrated circuits.

Accordingly, the interference spectrometry may use the poly silicon layer and the nitride layer as the two reflective surfaces required for interference spectroscopy.

The thickness of the poly silicon layer which should remain on the surface depends on the particular geometric conditions of the trench and the thickness of the poly silicon layer intended upon the bottom of the trench. In many typical applications, like the forming of capacitors, the etching will be stopped when the remaining poly silicon layer is between 10 and 30 nm thick.

The etching can e.g. be stopped when the remaining poly silicon layer is about 20 nm thick. This value has been proven to be useful in the manufacturing of capacitors in DRAM structures.

The thickness of the layer correlates with the values determined by interference spectroscopy. The correlation does not need to be calculated, but may be determined experimentally. For this purpose, the etching of samples is stopped, their values for spectrometry is determined, and a cross section of same is subjected to electron microscopy, where the thickness of the poly silicon layer can easily be determined. Through this approach, the spectroscopic value for a particular thickness can easily be determined.

The wavelength of the emitted light depends on the use of a particular model of spectrometer and the concrete application. A wavelength of 257 nm was found to be suitable for most applications.

The recess etch step gives the poly silicon layer its final thickness and shape. Therefore, it must fulfil particular requirements. The inventors have found out that the recess etching is advantageously performed using hydrogen bromide, chlorine. The etching atmosphere may preferably be diluted with a helium/oxygen mixture or any other comparable inert gas or gas mixture having similar properties. Due to the effect of microloading, one gets a higher etch rate within the trench, compared to the overfill areas (areas on top of the nitride). This beneficial effect results in the desired, substantially planar surface of the finished poly silicon layer within the trench, since it compensates for the initially bulged periphery of the poly silicon material at the trench.

The first etch step using SF6/CF4 provides for a substantially planar surface on top of the wafer. Softlanding is performed by in-situ measurement employing interference spectrometry. The substantially planar surface which is achieved

by the above mentioned etch gases has a slight recess within the trench area. The switch to Cl2/HBr etch gases for the trench etch has microtrenching properties so that the etching behaviour near the sidewalls of the trench is faster than the etching in the centre of the trench. As a result, the trench is efficiently etched without leaving residues on the sidewalls of the trench leading to a substantially planar surface at the bottom of the trench.

The trench formed with the present invention might e.g. form part of a capacitor. The manufacturing of a capacitor is in fact a very preferred application of the present invention and was the initial reason for the inventor's search for improving the planarization and the recess process.

It is further on preferred that the poly silicon layer is deposited onto the integrated circuit by a low pressure chemical vapour deposition step.

In the following, the invention will be further explained and detailed. Reference will be taken to the figures, in which:

Fig.1 shows the inventive process for planarization;

Fig. 2 shows an electron microscopy photographs of a trench made by a prior art process in several stages of manufacturing; and

Fig. 3 shows an electron microscopy photographs of a trench made by the inventive process in several stages of manufacturing.

In the present invention, the hitherto employed step of CMP for planarizing has been replaced by an etch step which can easily be integrated into the whole manufacturing process of integrated circuits. The progress of etching the poly silicon layer is preferably monitored by measuring its remaining thickness. Finally, the poly silicon in the trenches is removed by recess etching until only a substantially planar poly silicon layer within the trenches remains.

Fig. 1 schematically illuminates the inventive process by showing the consecutive stages of a silicon surface viewed in cross section. Fig. 1 A shows the initial state of the surface before any poly silicon is deposited onto it. The silicon 1 containing the circuit structures is overlayed by a nitride layer 2. Through both layers extend the trenches 3, e.g. deep trenches for capacitors. As shown in Fig. 1 B, the entire surface of the integrated circuits, i.e. the wafer, is then covered with a poly silicon layer 4 (called an "overfill" outside the trenches) which also fills the trenches 3 with a plug 5.

The inventive process starts with a first etch step. This process step may be typically run at a pressure of 0,4 Pascal with a source power of about 1500 W and a bias power of about 120 W. As etch gases, CF4 and SF6 are used. The flow rate for CF_4 may e.g. be from 40 to 60 sccm (standard cubic centimeters per minute), e.g. 52 sccm, while the flow rate for SF_6 could preferably be 30 to 50 sccm, e.g. 43 sccm. The process time will under such conditions preferably be about 30 seconds. These parameters may however be varied according to the general knowledge of a person skilled in the art. The result of the first etch step is shown in Fig. 1 C. The thickness of the poly silicon overfill layer 4 has been substantially re-

duced, while the plugs remain unchanged. However, depending on the particular formation of the process, also a portion of the plugs 5 could be removed at the first etch step. When the etching has led to the result shown in Fig. 1 C, the etch step is stopped, and a further etch step, a recess etching with microtrenching properties is started which removes portions of the plugs 5. Conditions for this process may typically comprise a pressure of 0,53 Pascal at a source power of about 960 W and a bias power of about 240 W. The flow rate for Cl_2 may e.g. be 135 sccm, the flow rate for HBr may preferably be 40 to 50 sccm, e.g. 45 sccm, and the flow rate for He/O_2 may preferably be 10 to 25 sccm, e.g. 16 sccm. The process time will under such conditions preferably be about 30 seconds. Variations of these parameters are possible and will be contemplated by skilled persons. The result of this etch step is shown in Fig. 1 D. In this example, the poly silicon layer 4 was removed altogether, as preferred. Alternatively, a very thin poly silicon overfill layer may still remain on nitride layer 2.

The integrated planarisation and recess etch process according to the invention can be performed within the same etch chamber with an in-situ measurement capability, preferably interferometric spectrometry by simply switching the etch chemistry in response to a signal from the interferometric spectrometry measurement device. The integrated etch process can be performed within the same chamber without breaking the vacuum.

The plugs 5 are also eroded, while a substantially planar surface of the plug is formed. This lead to a recess 6 having the desired depth within the trench. In the example shown, the plug is no longer in contact with the nitride layer 2.

This however, may depend on the concrete embodiment and the requirements and kinds of the manufactured trenches.

Fig. 2 shows photographs of an electron microscopy of cross sections of material treated according to prior art processes. In Fig. 2 A, there is shown a wafer close to its surface after the poly silicon layer has been deposited and prior to planarization. In this photograph, the surface runs from the middle of the upper edge to the middle of the right edge. The same reference numerals indicate the same structures as in Fig, 1.

Fig. 2 B which is rotated relative to Fig. 2 A, shows the surface of the wafer after the CMP step. The poly silicon overfill is completely removed, while the plugs 5 still remain in the trenches. In Fig. 2 C, finally, the end product after the etching is shown. As can be recognised from the figure, the trench 3 shows a niche in the silicon layer 1 where it confronts the nitride layer 2.

Fig. 3 shows an example for trenches manufactured according to the invention. Fig. 3 A corresponds to Fig. 2 A. Fig. 3 B shows the surface of the wafer after the first etching step. As can be seen, there is still a thin poly silicon overfill layer 4 overlaying the nitride layer 2. After the second etching, the recess etch step, the recesses 6 are formed and the poly silicon overfill layer 4 is completely removed, as can be seen from Fig. 3 C. These recesses 6 show smoother walls then the recesses produced by the prior art CMP process.

The process according to the invention allows for the production of recesses, e.g. in capacitor trenches, with integrated

circuits. The invention is particularly useful as an integrated planarization process for low aspect ratio recess etching. The inventive process results in a reduction of cycle time due to the integrated processing made possible. The total production and tool cost is reduced by eliminating the unfavourable CMP step. Further, no tool modifications are required, so that available resources can be used.

Claims

1. Process for forming a recess in at least one poly silicon overfilled trench in an integrated circuit, comprising the following steps:

- uniformly etching the poly silicon overfill layer (4) using a gas mixture comprising SF6 and CF4;

- stopping the etching before the poly silicon layer (4) is completely removed from the surface of the integrated circuit; and

- recess etching the poly silicon layer (4) with microtrenching properties using a gas mixture comprising hydrogen bromine and chlorine for forming a substantially planar recess (6) near the top of the at least one trench (3).

2. Process according to claim 1, characterised in that the etching comprises a plasma etching.

3. Process according to claim 1 or 2, characterised in that the stopping of the etching is decided based on measuring the layer thickness of the poly silicon layer (4).

4. Process according to claim 3,characterized in that the thickness of the poly silicon layer (4) is measured by interference spectrometry.

5. Process according to any of claims 1 to 4, characterised in that a nitride layer (2) is interposed between the silicon (1) of the integrated circuit and the poly silicon layer (4).

6. Process according to claim 5, characterised in that the interference spectrometry uses the poly silicon layer (4) and the nitride layer (2).

7. Process according to any of claim 1to 6, characterised in that the etching is stopped when the remaining poly silicon layer (4) is between 10 and 30 nm thick.

8. Process according to claim 7, characterised in that the etching is stopped when the remaining poly silicon layer (4) is about 20 nm thick

9. Process according to any of claims 1 to 8, characterised in that the recess etching is performed using a helium/oxygen mixture.

10. Process according to any of claims 1 to 9, characterised in that the trench (3) is part of a capacitor.

11. Process according to any of claims 1 to 10, characterised in that the poly silicon layer (4) is deposited onto the integrated circuit by a low pressure chemical vapour deposition process.

12. Process according to any of claims 1 to 11, characterized in that the step of etching the poly silicon overfill layer (4) and the step of recess etching the poly silicon layer (4) are performed within the same etch chamber, preferably without breaking the vacuum.

FIG 1A

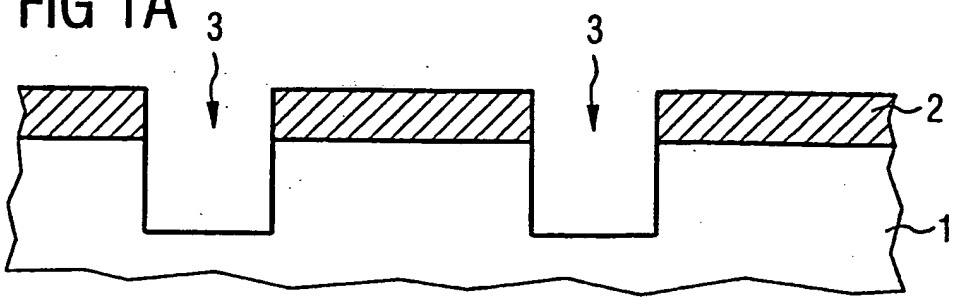


FIG 1B

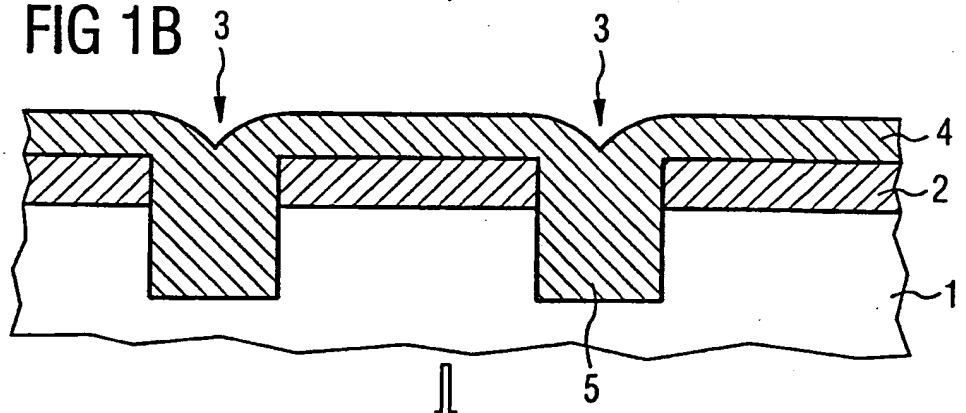


FIG 1C

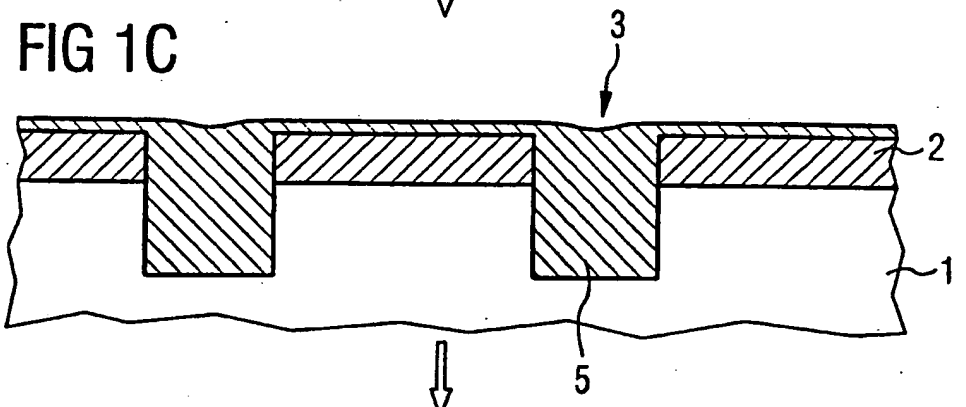


FIG 1D

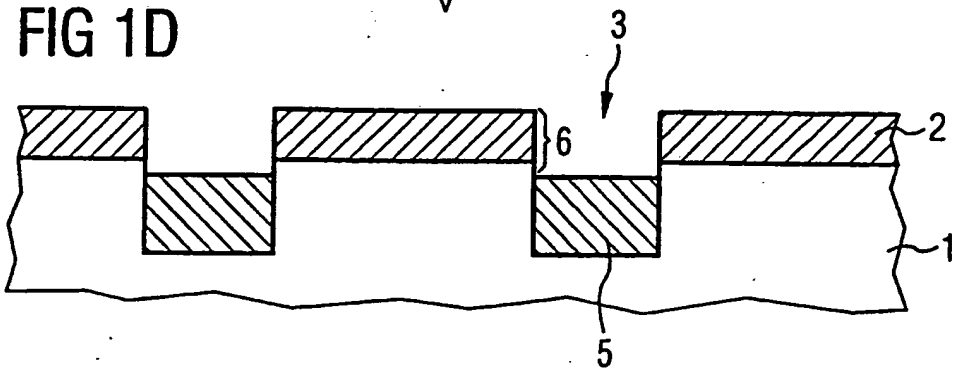


FIG 2A
PRIOR ART

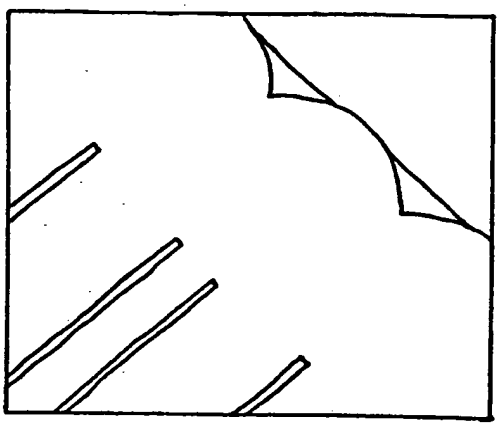


FIG 2B
PRIOR ART

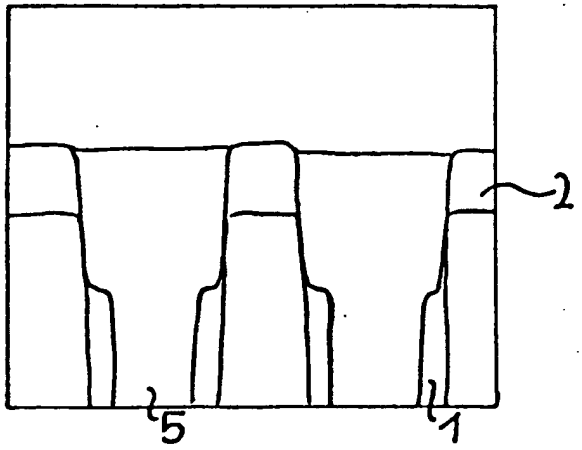


FIG 2C
PRIOR ART

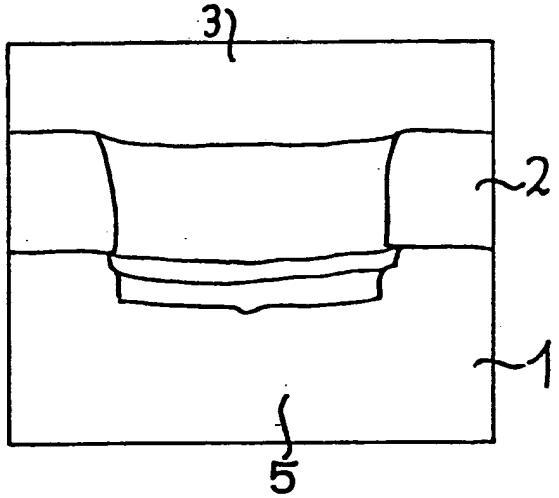


FIG 3A

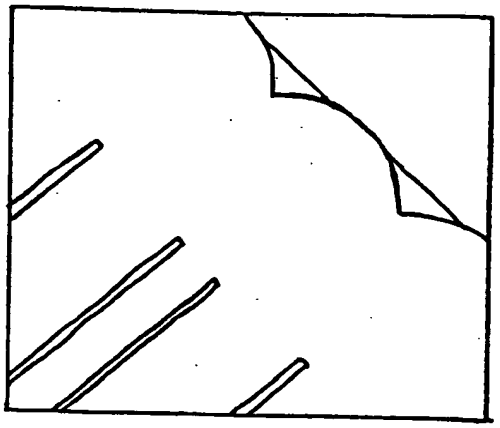


FIG 3B

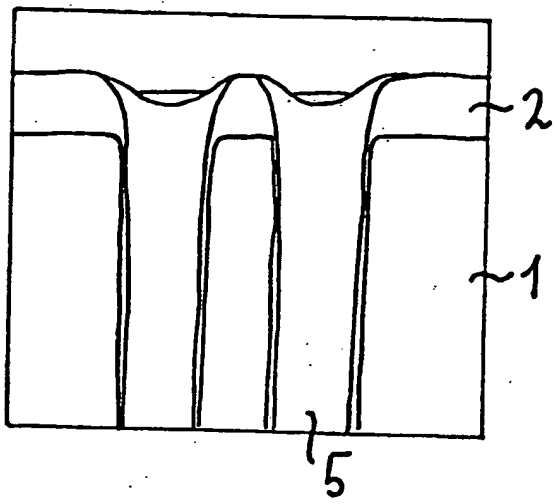
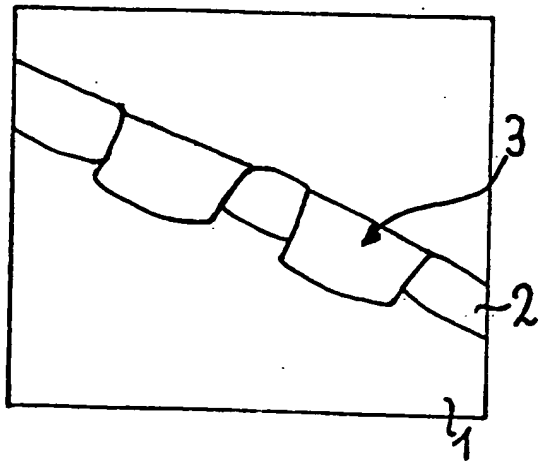


FIG 3C



INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/3213 H01L27/108 H01L21/763 H01L21/8242

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, PAJ, EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 905 758 A (SIEMENS AG) 31 March 1999 (1999-03-31) column 2, line 5 - line 45; figures 1-3 column 2, line 57 -column 3, line 14 column 4, line 1 - line 19 column 5, line 19 - line 32; figures 8,9 column 6, line 11 - line 25; table 1 --- -/--	1,2,5, 9-11

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2001	08/05/2001

Name and mailing address of the ISA	Authorized officer
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PCT/EP 01/00715

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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